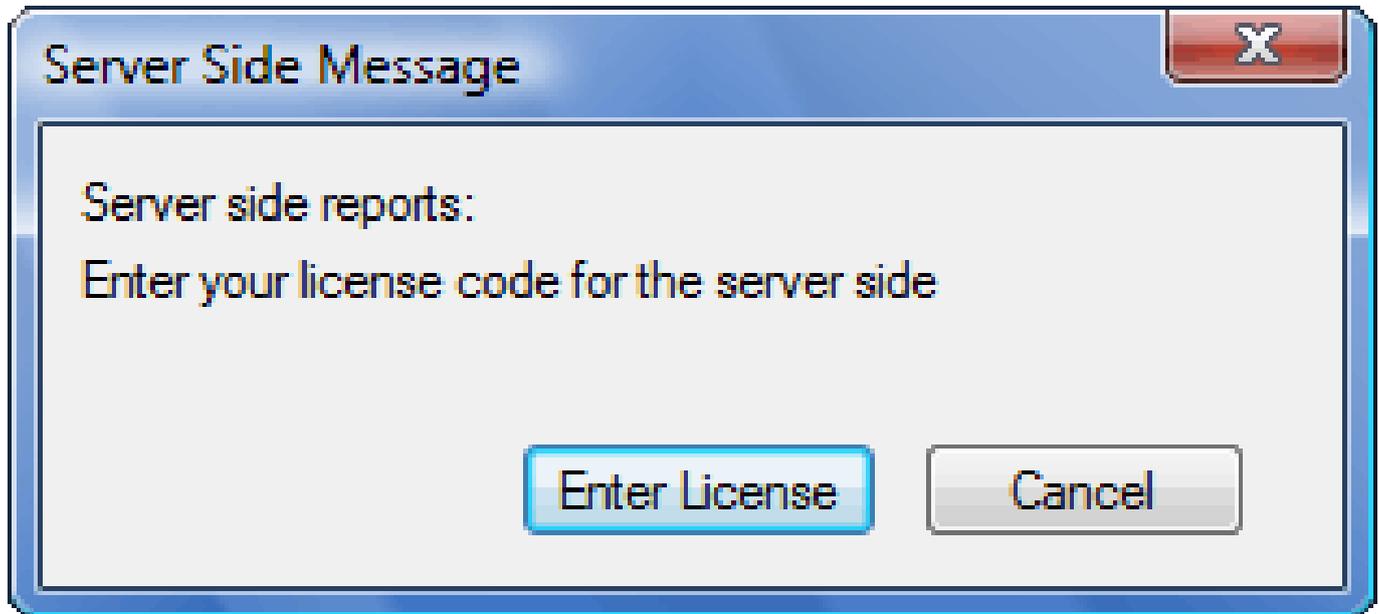

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Chasse-Alouette Theme Manager 3.2.1.2 Full Version Download HP LaserJet 5550 driver manual download Mavericks
Crossover Windows 10 download1. Field of the Invention The present invention relates to a single crystal substrate for a
semiconductor device. 2. Description of the Background Art In recent years, semiconductor devices have been advanced to be
smaller and higher in integration, and semiconductor devices such as ICs, LSIs, and the like have been made smaller and higher
in integration in association with the advance of device miniaturization. On the other hand, with the advance of integration, the
number of pins per chip is increased and a high-density package structure has been adopted, and a chip size has been reduced.
As a result, the number of pins is increased and the distance between the pins is narrowed. In association with the advance of
device miniaturization, the pitch of interconnections is reduced and wiring pitches are narrowed, and wirings and
interconnections on the surface of a semiconductor substrate are made finer. Due to this, an issue has arisen that noise and
crosstalk are caused between wirings and wirings are electromagnetically induced to malfunction. As a countermeasure against
this issue, a structure in which a via hole reaching an interconnection layer is formed in the surface of a semiconductor substrate
is adopted. The via hole is formed on the surface of the semiconductor substrate by using a lithographic technique, and an
interconnection layer is formed in the via hole, whereby a plurality of interconnections which are independent of each other are
formed. The distance between the interconnections is increased and the electromagnetic induction between the interconnections
is reduced, and it is thereby possible to effectively prevent the malfunction. Japanese Patent Laying-Open No. 9-232465 (Patent
Document 1) discloses a semiconductor device in which a concave portion is formed in a conductive layer. The via hole formed
in a semiconductor substrate is covered with a conductive layer. Japanese Patent Laying- 82157476af

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